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| 10/677,601 | 10/02/2003 | Eung-Soo Kim | LEPA121686 | 8228 |

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| EXAMINER |
|---|
| GOFF II, JOHN L |

| ART UNIT | PAPER NUMBER |
|---|---|
| 1733 | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

RJ

| *Office Action Summary* | Application No.<br>10/677,601 | Applicant(s)<br>KIM ET AL. | |
|---|---|---|---|
| | Examiner<br>John L. Goff | Art Unit<br>1733 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 December 2005*.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12* is/are pending in the application.
4a) Of the above claim(s) *4 and 5* is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-3 and 6-12* is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on *20 December 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a)☒ All b)☐ Some * c)☐ None of:
1.☒ Certified copies of the priority documents have been received.
2.☐ Certified copies of the priority documents have been received in Application No. _____.
3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date *10/2/03*.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election of Species I, readable on claims 1-3 and 6-12, in the reply filed on 12/2/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

### *Drawings*

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 101 on page 4, line 17, 506 on page 22, line 11, 607a on page 22, line 13, and 607b on page 22, line 13. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 207 in Figure 2E.

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 112*

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 9 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 9 recites the limitation "the via holes of the circuit layers with the openings of the insulating layers" in lines 3-5. There is insufficient antecedent basis for this limitation in the claim. Independent claim 1 neither requires the circuit layers to include via holes nor the insulating layers to include openings (these limitations are required however in dependent claims 2, 3, 6, and 7). It is suggest applicants delete from claim 9 "the via holes of the circuit layers

with the openings of the insulating layers" and insert therein - - the circuit layers with the insulating layers - - to overcome the rejection.

### *Claim Rejections - 35 USC § 102*

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 2, 7, and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakatani et al. (U.S. Patent 5,484,647).

Nakatani et al. disclose a method of manufacturing a multilayered printed circuit board (Column 1, lines 8-12). Nakatani et al. teach forming a double-sided printed circuit board by providing a copper clad laminate (CCL), creating via holes in the CCL, copper-plating the CCL and walls of the via holes, and forming circuit patterns on both sides of the CCL (Figures 3 and 4 and Column 15, lines 41-67, Column 16, lines 1-9 and 54-67 and Column 17, lines 1-38). Nakatani et al. teach forming an insulating layer by providing a prepreg including attached release films, creating openings in the prepreg, plugging paste in the openings, and removing the release films (Figures 1A to 1C, 3, and 4 and Column 13, lines 61-67 and Column 14, lines 1-17 and Column 15, lines 61-67). Nakatani et al. teach forming the multilayered printed circuit board in a single step by providing a plurality of double-sided printed circuit boards, providing a plurality of insulating layers, alternately layering the double-sided printed circuit boards and insulating layers, and compressing the double-sided printed circuit boards and insulating layers in a heated press in a single step (Figures 3 and 4 and Column 16, lines 54-57 and Column 17, lines 24-28 and Column 18, lines 17-24). Alternatively, Nakatani et al. teach forming the multilayered printed circuit board in a build-up process by providing a double-sided printed circuit board, providing two insulating layers, placing the double-sided printed circuit board between the insulating layers, compressing the double-sided printed circuit board and insulating layers in a heated press, and then repeating the above steps for a needed number of times to add any desired number of additional double-sided circuit boards and insulating layers (Figures 3 and 4 and Column 16, lines 54-57 and Column 17, lines 24-28 and Column 18, lines 17-24).

### *Claim Rejections - 35 USC § 103*

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 1-3, 6, 7, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (Figures 1A-1M and Specification Pages 1-10) in view of Nakatani et al.

The admitted prior art discloses a method of manufacturing a multilayered printed circuit board (Page 4, lines 5-15). The admitted prior art teaches forming a double-sided printed circuit board by providing a CCL, creating via holes in the CCL, copper-plating the CCL and walls of the via holes, plugging conductive paste into the via holes (it being noted this step is included or omitted depending upon the purpose of the finally formed multilayered circuit board), and forming circuit patters on both sides of the CCL (Figures 1A-1E and Page 5, lines 18-22 and Page 6, lines 13-24 and Page 7, lines 15-18). The admitted prior art teaches forming the multilayered printed circuit board in a build-up process by providing a double-sided printed circuit board, providing two insulating layers, placing the double-sided printed circuit board between the insulating layers, compressing the double-sided printed circuit board and insulating layers, and then repeating the above steps for a needed number of times to add any desired number of additional double-sided circuit boards and insulating layers (Figures 1F-1M and Page 4, lines 5-15 and Page 8, lines 18-23 and Page 10, lines 9-13). The admitted prior art is silent as to forming the multilayered printed circuit board in a single step process as opposed to a build-up process. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the admitted prior art to form the multilayered printed circuit board in a single step process as both single step and build-up processes were known equivalent multilayered printed circuit board forming processes in the art as shown by Nakatani et al. wherein the single step process would advantageously only require a single compressing step in a heated press using preformed circuit boards and insulating layers.

Regarding claim 7, as to forming the preformed insulating layers it is noted the finished insulating layers taught by the admitted prior art include conductive openings (Figures 1G-1M) such that it would have been obvious to one of ordinary skill in the art at the time the invention was made to use as the preformed insulating layers in the admitted prior art as modified by Nakatani et al. those formed by well known techniques in the art such as those shown for example by Nakatani et al. as only the expected results would be achieved.

Nakatani et al. is described above in full detail.

12. Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakatani et al. in view of the admitted prior art.

Nakatani et al. is described above in full detail. Nakatani et al. are silent as to plugging the copper-plated via holes with conductive paste, it being noted Nakatani et al. are not limited to forming multilayer circuit boards having any particular purpose. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include in Nakatani et al. a step of plugging the copper-plated via holes of the CCL with conductive paste depending upon the particular purpose of the multilayer circuit board as was well known in the art and shown for example by the admitted prior art.

The admitted prior art is described above in full detail.

13. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakatani et al. in view of Appelt et al. (U.S. Patent 5,928,970).

Nakatani et al. as applied above teach all of the limitations in claim 8 except for the insulating layer including an inner completely hardened (c-stage) resin layer between two semi-hardened (b-stage) resin layers. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use as the prepreg in the insulating layer taught by Nakatani et al. a prepreg having an inner completely hardened (c-stage) resin layer between two semi-hardened (b-stage) resin layers as was well known in the art as shown for example by Appelt et al. to prevent the generation of dust during fabrication and use of the insulating layer.

Appelt et al. show the well known technique of forming an insulating layer from a prepreg including an inner completely hardened (c-stage) resin layer between two semi-hardened (b-stage) resin layers to prevent generating dust during use of the insulating layer (Column 1, lines 20-25 and Column 2, lines 58-61).

14. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art and Nakatani et al. as applied to claims 1-3, 6, 7, and 11 above, and further in view of Appelt et al.

Claim 8 is rejected in the same manner as that applied above in paragraph 13.

15. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakatani et al. in view of Pomatto et al. (U.S. Patent 4,899,440).

Nakatani et al. as applied above teach all of the limitations in claims 9 and 10 except for a teaching of targeting and trimming the double-sided circuit boards and insulating layers to precisely match the via holes of the double-sided circuit boards with the openings of the insulating layers in the single step process. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakatani et al. to include well known finishing steps following formation of the double-sided circuit boards and insulating layers such as targeting and forming alignment holes and shearing the edges as shown for example by

Pomatto et al. to accurately orient, i.e. precisely match, the double-sided circuit boards and insulating layers prior to compressing into a multilayered circuit board.

Pomatto et al. disclose well known finishing steps following formation of double-sided circuit boards include targeting and forming alignment holes in the boards by x-ray drilling and shearing the edges of the boards, i.e. including removing any exuded and solidified resin, to allow accurately orienting the double-sided circuit boards in subsequent work operations (Column 1, lines 7-23 and 56-63).

16. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art and Nakatani et al. as applied to claims 1-3, 6, 7, and 11 above, and further in view of Pomatto et al.

Claims 9 and 10 are rejected in the same manner as that applied above in paragraph 15.

17. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakatani et al. in view of Ochi et al. (U.S. Patent 6,459,046) and JP 2295700 (See also the abstract).

Nakatani et al. as applied above teach all of the limitations in claim 12 except for a teaching of performing the heated compressing by pressing in a vacuum chamber using an electric heater. It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the heated compression taught by Nakatani et al. using a vacuum press as was well known and shown for example by Ochi et al. to compress and form the multilayered circuit board with a minimum of trapped air wherein the specific type of heated vacuum compression device would have been any of the well known heated vacuum compression devices in the art such as that shown for example by JP 2295700 including a vacuum chamber and an electric heater wherein only the expected results would be achieved.

Ochi et al. disclose a method of manufacturing a multilayered printed circuit board (Column 4, lines 21-25). Ochi et al. teach forming an insulating layer by providing a prepreg including attached release films, creating openings in the prepreg, plugging paste in the openings, and removing the release films (Figures 1A-E and Column 5, lines 36-67). Ochi et al. teach forming the multilayer printed circuit board in a build-up process by providing a double-sided printed circuit board, providing two insulating layers, placing the double-sided printed circuit board between the insulating layers, compressing the double-sided printed circuit board and insulating layers in a heated vacuum press, and then repeating the above steps for a needed number of times to add any desired number of additional double-sided circuit boards and insulating layers (Figures 3C and 3E and Column 8, lines 58-67 and Column 9, lines 1-30).

JP 2295700 is exemplary of a well known heated platen vacuum compression device wherein the device includes a vacuum chamber and an electric heater for providing the vacuum and heat during compression (See the abstract).

18. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art and Nakatani et al. as applied to claims 1-3, 6, 7, and 11 above, and further in view of Ochi et al. and JP 2295700.

Claim 12 is rejected in the same manner as that applied above in paragraph 17.

## ***Double Patenting***

19. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application

claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

> Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

20. Claims 1-3 and 6-12 are directed to an invention not patentably distinct from claim 1 of commonly assigned 10/717,977.

21. Claims 1 and 7 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/717,977. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 of copending Application No. 10/717,977 discloses a method of manufacturing a multilayered printed circuit board fully encompassing claims 1 and 7. Claim 1 of copending Application No. 10/717,977 teaches forming a printed circuit board by providing a copper stack plate (i.e. CCL), creating via holes in the plate, copper-plating the plate and walls of the via holes, and forming circuit patterns on the plate. Claim 1 of copending Application No. 10/717,977 teaches forming an insulating layer by providing an insulating layer including attached release films, creating via holes, i.e. openings, in the insulating material, plugging paste in the via holes, and removing the release films. Claim 1 of copending Application No. 10/717,977 teaches forming the multilayered printed circuit board in a single step by providing a

number of printed circuit boards, providing a number of insulating layers, alternately layering the circuit boards and insulating layers, and compressing the circuit boards and insulating layers.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

22. Claims 2, 3, and 6 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/717,977 in view of the admitted prior art. Claim 1 of copending Application No. 10/717,977 is described above. Claim 1 of copending Application No. 10/717,977 does not specifically teach forming double-sided circuit boards. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form as the circuit boards in claim 1 of copending Application No. 10/717,977 double-sided circuit boards as was well known and shown for example by the admitted prior art as only the expected results would be achieved. Claim 1 of copending Application No. 10/717,977 does not teach plugging the copper-plated via holes with conductive paste. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include in claim 1 of copending Application No. 10/717,977 a step of plugging the copper-plated via holes of the plate with conductive paste depending upon the particular purpose of the multilayer circuit board as was well known in the art and shown for example by the admitted prior art. The admitted prior art is described above in full detail.

This is a provisional obviousness-type double patenting rejection.

23. Claim 8 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/717,977 in view of Appelt et al. Claim 1 of copending Application No. 10/717,977 is described above. Claim 1

of copending Application No. 10/717,977 does not teach the insulating layer as including an inner completely hardened (c-stage) resin layer between two semi-hardened (b-stage) resin layers. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use as the insulating material in the insulating layer taught by claim 1 of copending Application No. 10/717,977 an insulating material having an inner completely hardened (c-stage) resin layer between two semi-hardened (b-stage) resin layers as was well known in the art as shown for example by Appelt et al. to prevent generation of dust during fabrication and use of the insulating layer. Appelt et al. is described above in full detail.

This is a provisional obviousness-type double patenting rejection.

24. Claims 9 and 10 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/717,977 in view of Pomatto et al. Claim 1 of copending Application No. 10/717,977 is described above. Claim 1 of copending Application No. 10/717,977 does not teach targeting and trimming the circuit boards and insulating layers to precisely match the via holes of the circuit boards with the openings of the insulating layers. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify claim 1 of copending Application No. 10/717,977 to include well known finishing steps following formation of the circuit boards and insulating layers such as targeting and forming alignment holes and shearing the edges as shown for example by Pomatto et al. to accurately orient, i.e. precisely match, the circuit boards and insulating layers prior to compressing into a multilayered circuit board. Pomatto et al. is described above in full detail.

This is a provisional obviousness-type double patenting rejection.

25. Claims 11 and 12 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/717,977 in view of Ochi et al. and JP 02295700. Claim 1 of copending Application No. 10/717,977 is described above. Claim 1 of copending Application No. 10/717,977 does not teach compressing in a vacuum chamber using an electric heater. It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the compression taught by claim 1 of copending Application No. 10/717,977 using a heated vacuum press as was well known and shown for example by Ochi et al. to compress the multilayered circuit board with a minimum of trapped air wherein the type of heated vacuum compression device would have been any of the well known heated vacuum compression devices in the art such as that shown for example by JP 2295700 including a vacuum chamber and an electric heater wherein only the expected results would be achieved. Ochi et al. and JP 02295700 are described above in full detail

This is a provisional obviousness-type double patenting rejection.

26. The U.S. Patent and Trademark Office normally will not institute an interference between applications or a patent and an application of common ownership (see MPEP § 2302). Commonly assigned 10/717,977, discussed above, would form the basis for a rejection of the noted claims under 35 U.S.C. 103(a) if the commonly assigned case qualifies as prior art under 35 U.S.C. 102(e), (f) or (g) and the conflicting inventions were not commonly owned at the time the invention in this application was made. In order for the examiner to resolve this issue, the assignee can, under 35 U.S.C. 103(c) and 37 CFR 1.78(c), either show that the conflicting

inventions were commonly owned at the time the invention in this application was made, or name the prior inventor of the conflicting subject matter.

A showing that the inventions were commonly owned at the time the invention in this application was made will preclude a rejection under 35 U.S.C. 103(a) based upon the commonly assigned case as a reference under 35 U.S.C. 102(f) or (g), or 35 U.S.C. 102(e) for applications pending on or after December 10, 2004.

27. Claims 1-3 and 6-12 are directed to an invention not patentably distinct from claims 1, 3, and 6 of commonly assigned 10/948,875.

28. Claims 1 and 2 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 3, and 6 of copending Application No. 10/948,875. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1, 3, and 6 of copending Application No. 10/948,875 disclose a method of manufacturing a multilayered printed circuit board fully encompassing claims 1 and 2. Claims 1, 3, and 6 of copending Application No. 10/948,875 teach forming a double-sided printed circuit board by providing a CCL, creating via holes in the CCL, copper-plating the CCL and walls of the via holes, and forming circuit patterns on the CCL. Claims 1, 3, and 6 of copending Application No. 10/948,875 teach forming the multilayered printed circuit board in a single step by providing a number of printed circuit boards, providing a number of insulating layers, alternately layering the circuit boards and insulating layers, and compressing the circuit boards and insulating layers.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

29. Claims 3 and 6 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 3, and 6 of copending Application No. 10/948,875 in view of the admitted prior art. Claims 1, 3, and 6 of copending Application No. 10/948,875 are described above. Claims 1, 3, and 6 of copending Application No. 10/948,875 do not teach plugging the copper-plated via holes with conductive paste. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include in claims 1, 3, and 6 of copending Application No. 10/948,875 a step of plugging the copper-plated via holes of the plate with conductive paste depending upon the particular purpose of the multilayer circuit board as was well known in the art and shown for example by the admitted prior art. The admitted prior art is described above in full detail.

This is a provisional obviousness-type double patenting rejection.

30. Claim 7 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 3, and 6 of copending Application No. 10/948,875 in view of Ochi et al. Claims 1, 3, and 6 of copending Application No. 10/948,875 are described above. Claims 1, 3, and 6 of copending Application No. 10/948,875 are silent as to using the claimed insulating layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use as the insulating layer in claims 1, 3, and 6 of copending Application No. 10/948,875 the insulating layer taught by Ochi et al. for providing the multilayer circuit board with insulating layers having conductive paths. Ochi et al. is described above in full detail.

This is a provisional obviousness-type double patenting rejection.

31. Claim 8 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 3, and 6 of copending Application No. 10/948,875 in view of Appelt et al. Claims 1, 3, and 6 of copending Application No. 10/948,875 is described above. Claims 1, 3, and 6 of copending Application No. 10/948,875 do not teach the insulating layer as including an inner completely hardened (c-stage) resin layer between two semi-hardened (b-stage) resin layers. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use as the insulating material in the insulating layer taught by claims 1, 3, and 6 of copending Application No. 10/948,875 an insulating material having an inner completely hardened (c-stage) resin layer between two semi-hardened (b-stage) resin layers as was well known in the art as shown for example by Appelt et al. to prevent generating dust during fabrication and use of the insulating layer. Appelt et al. is described above in full detail.

This is a provisional obviousness-type double patenting rejection.

32. Claims 9 and 10 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 3, and 6 of copending Application No. 10/948,875 in view of Pomatto et al. Claims 1, 3, and 6 of copending Application No. 10/948,875 is described above. Claims 1, 3, and 6 of copending Application No. 10/948,875 are silent as to targeting and trimming the circuit boards and insulating layers to precisely match the via holes of the circuit boards with the openings of the insulating layers. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify claims 1, 3, and 6 of copending Application No. 10/948,875 to include well known finishing steps following formation of the double-sided circuit boards and insulating layers such as targeting and forming alignment holes and shearing the edges as shown for example by Pomatto et al. to

accurately orient, i.e. precisely match, the double-sided circuit boards and insulating layers prior to compressing into a multilayer circuit board. Pomatto et al. is described above in full detail.

This is a provisional obviousness-type double patenting rejection.

33. Claims 11 and 12 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 3, and 6 of copending Application No. 10/948,875 in view of Ochi et al. and JP 02295700. Claims 1, 3, and 6 of copending Application No. 10/948,875 are described above. Claims 1, 3, and 6 of copending Application No. 10/948,875 are silent as to compressing in a vacuum chamber using an electric heater. It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the heated compression taught by claims 1, 3, and 6 of copending Application No. 10/948,875 using a heated vacuum press as was well known and shown for example by Ochi et al. to compress the multilayer circuit board with a minimum of trapped air wherein the type of heated vacuum compression device would have been any of the well known heated vacuum compression devices in the art such as that shown for example by JP 2295700 including a vacuum chamber and an electric heater wherein only the expected results would be achieved. Ochi et al. and JP 02295700 are described above in full detail.

This is a provisional obviousness-type double patenting rejection.

34. The U.S. Patent and Trademark Office normally will not institute an interference between applications or a patent and an application of common ownership (see MPEP § 2302). Commonly assigned 10/948,875, discussed above, would form the basis for a rejection of the noted claims under 35 U.S.C. 103(a) if the commonly assigned case qualifies as prior art under 35 U.S.C. 102(e), (f) or (g) and the conflicting inventions were not commonly owned at the time

the invention in this application was made. In order for the examiner to resolve this issue, the assignee can, under 35 U.S.C. 103(c) and 37 CFR 1.78(c), either show that the conflicting inventions were commonly owned at the time the invention in this application was made, or name the prior inventor of the conflicting subject matter.

A showing that the inventions were commonly owned at the time the invention in this application was made will preclude a rejection under 35 U.S.C. 103(a) based upon the commonly assigned case as a reference under 35 U.S.C. 102(f) or (g), or 35 U.S.C. 102(e) for applications pending on or after December 10, 2004.

## *Conclusion*

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **John L. Goff** whose telephone number is **(571) 272-1216**. The examiner can normally be reached on M-F (7:15 AM - 3:45 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Crispino can be reached on (571) 272-1226. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John L. Goff